

SGP-QSFP+ER

40Gb/s QSFP+ ER4 40KM Fiber Transceiver

Features

Compliant with 40G Ethernet IEEE802.3ba and 40GBASE-ER4 Standard

QSFP+ MSA compliant

Compliant with QDR/DDR Infiniband data rates

Up to 11.2Gb/s data rate per wavelength

4 CWDM lanes MUX/DEMUX design

Up to 40km transmission on single mode fiber (SMF)

18.5dB link insertion loss budget

Operating case temperature: 0 to 70°C

Maximum power consumption 3.5W

LC duplex connector

RoHS compliant

Applications

40GBASE-ER4 Ethernet Links

Infiniband QDR and DDR interconnects

Client-side 40G Telecom connections

1. General Description

SGP-QSFP-ER is a transceiver module designed for 40km optical communication applications. The design is compliant to 40GBASE-ER4 of the IEEE P802.3ba standard. The module converts 4 inputs channels (ch) of 10Gb/s electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 40Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 40Gb/s input into 4 CWDM channels signals, and converts them to 4 channel output electrical data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. It contains a duplex LC connector for the optical

interface and a 148-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module.

FLD-QSFP-ER4-40 is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP+ Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

2. Functional Description

SGP-QSFP-ER converts the 4-channel 10Gb/s electrical input data into CWDM optical signals (light), by a driven 4-wavelength Distributed Feedback Laser (DFB) array. The light is combined by the MUX parts as a 40Gb/s data, propagating out of the transmitter module from the SMF. The receiver module accepts the 40Gb/s CWDM optical signals input, and de-multiplexes it into 4 individual 10Gb/s channels with different wavelength. Each wavelength light is collected by a discrete avalanche photodiode (APD), and then outputted as electric data after amplified first by a TIA and then by a post amplifier. Figure 1 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP+ memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground though a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. “Low” indicates a possible operational fault or a status critical to the host

system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

3. Transceiver Block Diagram

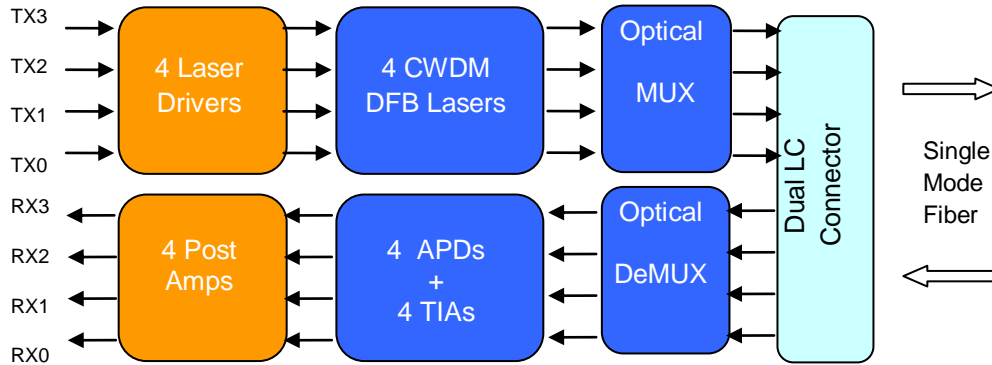


Figure 1. Transceiver Block Diagram

4. Pin Assignment and Description

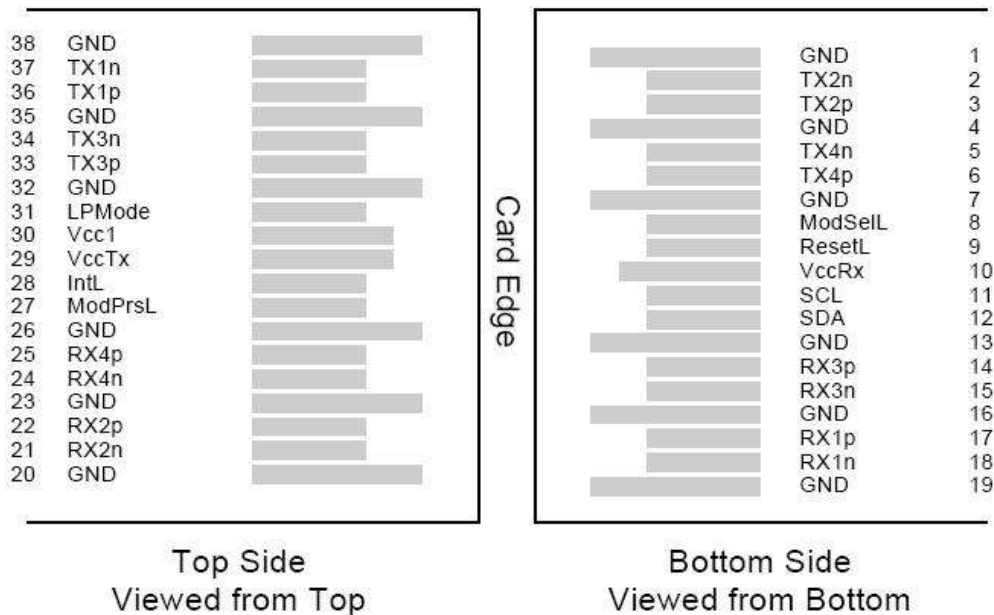


Figure 2. MSA compliant Connector

5. Pin Definitions

PIN	Logic	Symbol	Name/Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T _S	-40	85	degC	
Operating Case Temperature	T _{OP}	0	70	degC	
Power Supply Voltage	V _{CC}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	
Damage Threshold, each Lane	TH _d	3.8		dBm	

7. Recommended Operating Conditions and Power Supply Requirements

Parameter	Symbol	Min	Typical	Max	Units
Operating Case Temperature	T _{OP}	0		70	degC
Power Supply Voltage	V _{CC}	3.135	3.3	3.465	V
Data Rate, each Lane			10.3125	11.2	Gb/s
Control Input Voltage High		2		V _{CC}	V
Control Input Voltage Low		0		0.8	V
Link Distance with G652	D			40	km

8. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Power Consumption				3.5	W	
Supply Current	I _{CC}			1.1	A	
Transceiver Power-on Initialization Time				2000	ms	1
Transmitter (each Lane)						
Single-ended Input Voltage Tolerance (Note 2)		-0.3		4.0	V	Referred to TP1 signal common
AC Common Mode Input Voltage Tolerance		15			mV	RMS
Differential Input Voltage Swing Threshold		50			mV _{pp}	LOSA Threshold
Differential Input Voltage	V _{in,pp}	190		700	mV _{pp}	

Swing						
Differential Input Impedance	Zin	90	100	110	Ohm	
Differential Input Return Loss		See IEEE 802.3ba 86A.4.11			dB	10MHz- 11.1GHz
J2 Jitter Tolerance	Jt2	0.17			UI	
J9 Jitter Tolerance	Jt9	0.29			UI	
Data Dependent Pulse Width Shrinkage (DDPWS) Tolerance		0.07			UI	
Eye Mask Coordinates {X1, X2 Y1, Y2}		0.11, 0.31 95, 350			UI mV	Hit Ratio = 5x10 ⁻⁵
Receiver (each Lane)						
Single-ended Output Voltage		-0.3		4.0	V	Referred to signal common
AC Common Mode Output Voltage				7.5	mV	RMS
Differential Output Voltage Swing	Vout,pp	300		850	mVpp	
Differential Output Impedance	Zout	90	100	110	Ohm	
Termination Mismatch at 1MHz				5	%	
Differential Output Return Loss		See IEEE 802.3ba 86A.4.2.1			dB	10MHz- 11.1GHz
Common Mode Output Return Loss		See IEEE 802.3ba 86A.4.2.2			dB	10MHz- 11.1GHz
Output Transition Time		28			ps	20% to 80%
J2 Jitter Output	Jo2			0.42	UI	
J9 Jitter Output	Jo9			0.65	UI	
Eye Mask Coordinates {X1, X2		0.29, 0.5 150, 425			UI mV	Hit Ratio = 5x10 ⁻⁵

Y1, Y2}				
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Notes:

1. Power-on Initialization Time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the module is fully functional.
2. The single ended input voltage tolerance is the allowable range of the instantaneous input signals.

9. Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Wavelength Assignment	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Transmitter						
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	P _T			10.5	dBm	
Average Launch Power, each Lane	P _{AVG}	-2.7		4.5	dBm	
Optical Modulation Amplitude (OMA), each Lane	P _{OMA}	0.3		5.0	dBm	1
Difference in Launch Power between any Two Lanes (OMA)	P _{Tx,diff}			4.7	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-0.5			dBm	
TDP, each Lane	TDP			2.6	dB	
Extinction Ratio	ER	5.5			dB	
Relative Intensity Noise	RIN			-128	dB/Hz	12dB reflection
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	R _T			-12	dB	

Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.25,0.4,0.45,0.25,0.28,0.4}				
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Receiver						
Damage Threshold, each Lane	TH _d	3.8			dBm	2
Average Receive Power, each Lane		-21.2		-4.5	dBm	
Receiver Reflectance	R _R			-26	dB	
Receive Power (OMA), each Lane				-4	dBm	
Receiver Sensitivity (OMA), each Lane	SEN			-19	dBm	
Stressed Receiver Sensitivity (OMA), each Lane				-16.8	dBm	3
Difference in Receive Power between any Two Lanes (OMA)	Prx,diff			7	dB	
LOS Assert	LOSA	-35			dBm	
LOS Deassert	LOSD			-20	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Receiver Electrical 3 dB upper Cutoff Frequency, each Lane	Fc			12.3	GHz	
Conditions of Stress Receiver Sensitivity Test (Note 4)						
Vertical Eye Closure Penalty, each Lane			2.2		dB	
Stressed Eye J2 Jitter, each Lane			0.3		UI	
Stressed Eye J9 Jitter, each Lane			0.47		UI	

Notes:

1. Even if the TDP < 0.8 dB, the OMA min must exceed the minimum value specified here.

2. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
3. Measured with conformance test signal at receiver input for BER = 1×10^{-12} .
4. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

10. Digital Diagnostic Functions

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	+3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI_VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/- 1 dB fluctuation, or a +/- 3 dB total accuracy.

11. Mechanical Dimensions

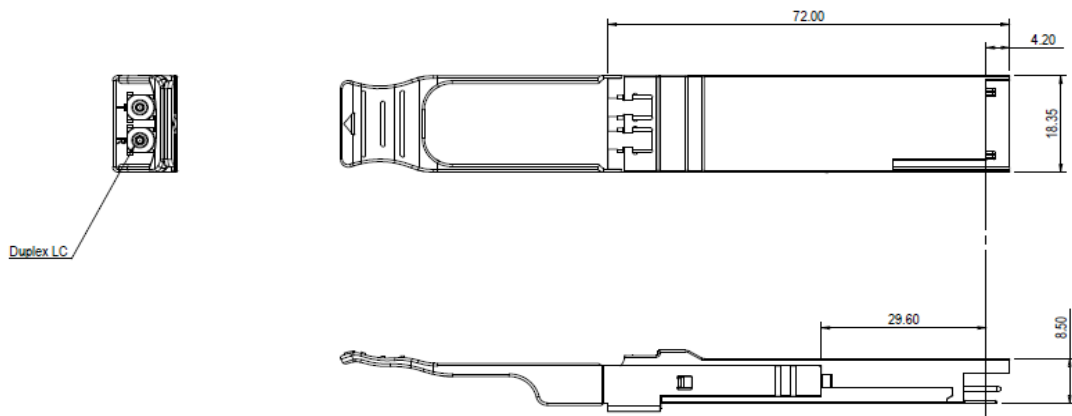


Figure 4. Mechanical Outline

12. ESD

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

13. Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).



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